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wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second deposited insulative layer along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate.

2. (amended) The MIS device of Claim 1, further comprising a gate adjacent to said first insulative layer and said second insulative layer within said trench.

3. (amended) The MIS device of Claim 2, wherein said gate comprises polysilicon.

4. (amended) The MIS device of Claim 1, further including a high conductivity region of said first conductivity type in said drain region adjacent to at least said bottom portion of said trench.

7. (amended) The MIS device of Claim 1, wherein said second insulative layer is a multi-layer insulative layer.

8. (amended) The MIS device of Claim 1, wherein said MIS device is a MOSFET.

9. (amended) A trench-gate device, comprising:

a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall,

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LAW OFFICES OF
SKIDMORE OWINGS & MERRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second deposited insulative layer along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer; whereby formation of said second insulative layer does not introduce substantial stress in said substrate; and

a gate adjacent to said first insulative layer and said second insulative layer within said trench.

10. (amended) The trench-gate device of Claim 9, wherein said gate comprises polysilicon.

11. (amended) The trench-gate device of Claim 9, further including a high conductivity region of said first conductivity type in said drain region adjacent to at least said bottom portion of said trench.

12. (amended) The trench-gate device of Claim 9, wherein said first insulative layer comprises an oxide.

13. (amended) The trench-gate device of Claim 9, wherein said second insulative layer comprises an oxide.

14. (amended) The trench-gate device of Claim 9, wherein said second insulative layer is a multi-layer insulative layer.

15. (amended) A trench-gate device, comprising:

a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

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Cont'd

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;

a second deposited insulative layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being in contact with said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate;

wherein a thickness of a transition insulative layer at the juncture of said first insulative layer and said second insulative layer is not less than a thickness of said first insulative layer; and

a gate adjacent to said first insulative layer and said second insulative layer within said trench.

16. (amended) The trench-gate device of Claim 15, further including a high conductivity region of said first conductivity type in said drain region adjacent to at least said bottom portion of said trench.

17. (amended) A trench-gate device, comprising:

a semiconductor substrate defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

LAW OFFICES OF
SILVERMAN MOORELL LLP

21 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 455-9000
FAX (408) 455-7879

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;

a second deposited insulative layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being in contact with said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate;

wherein a width of said trench at a vertical midpoint of said second insulative layer is not greater than a width of said trench adjacent to said body region; and

a gate adjacent to said first insulative layer and said second insulative layer within said trench.

18. (amended) The trench-gate device of Claim 17, further including a high conductivity region of said first conductivity type in said drain region adjacent to at least said bottom portion of said trench.

Please add Claims 30-31:

--30. The MIS device of Claim 1, wherein the first insulative layer is thermally grown.

31. The MIS device of Claim 9, where in the first insulative layer is thermally grown. --

LAW OFFICES OF
SKJERVEN MORRIS LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95119
(408) 433-7000
FAX (408) 433-7009